IMAGE DISPLAY SCREEN AND METHOD OF ADDRESSING SAID SCREEN

The invention concerns an image display screen and an addressing method for this screen.

In particular, the invention relates to a display screen of the type based on organic electroluminescent material with active matrix etched on amorphous silicon (a-Si).

Hydrogenated amorphous silicon thin film transistors exhibit advantages over polycrystalline silicon (p-Si) thin film transistors for the design of screens based on organic electroluminescent material since they are easier to fabricate and they exhibit uniform luminance on samples of relatively significant size.

However, the trigger threshold voltage of amorphous silicon transistors shifts over time during prolonged application of a voltage between their gate and their source.

This shift of trigger threshold voltages results in a process of marking of the image on the screen and changes in the screen's luminance over time.

There is known, in particular through document US 2003/052614, a screen of the abovementioned type including addressing control means intended, during each image frame, to apply to the current modulator of each light emitter of this screen and using one and the same circuit for addressing this light emitter, alternately, an addressing voltage representing an image datum and a voltage having an opposite polarity to the polarity of the addressing voltage.

However, this architecture and this driving mode are likely to bring about a lowering of the screen's luminance and a flicker effect on the screen, since the emission duration is reduced during each frame.

There is known, in particular through documents US 6 011 529 (see Figure 9 in particular) and WO 2004/051617, a screen of the abovementioned type including addressing control means intended, during each image frame, to apply to the current modulator of each light emitter of this screen and using at least one of the plurality of circuits for addressing this light emitter, an addressing voltage representing an image datum always having the same polarization.

The aim of the invention is to propose an alternative screen which exhibits low variations in luminance over time.

To this end, a subject of the invention is an image display screen including:

- light emitters distributed in rows of light emitters and columns of light emitters to form an array of light emitters,
- means for controlling the emissions of the light emitters of the array including:
  a) a first circuit for addressing a light emitter, associated with each light emitter of the array to control the current flowing through it, said circuit including:
     - a first current modulator intended to power said light emitter, said first modulator including a gate electrode and two current-carrying electrodes,
     - a first storage capacitor intended to set a potential at the gate electrode of the first current modulator,

b) for each light emitter, at least a second circuit for addressing a light emitter, said first and said second addressing circuits being associated in parallel with the same light emitter, said second circuit including:
- a second current modulator for said light emitter including a gate electrode and two current-carrying electrodes,
- a second storage capacitor intended to store a potential at the gate electrode of the second current modulator;

c) addressing control means intended to apply an addressing voltage at said first storage capacitor and at said second storage capacitor, said addressing voltage representing an image datum, and being intended to activate either the first or the second addressing circuit in order to supply current to the light emitter according to said image datum.

The screen is characterized in that the addressing control means are intended to set a bias voltage either at said first current modulator or at said second current modulator, said bias voltage having an opposite polarity to the polarity of said addressing voltage.

According to particular embodiments, the display screen includes one or more of the following characteristics:
- the addressing control means are intended to apply to said first current modulator first the addressing voltage to start a phase for activating the first addressing circuit, then the bias voltage to start a phase for biasing the first addressing circuit;
- the addressing control means are intended to apply to said second current modulator first the addressing voltage to start a phase for activating

the second addressing circuit, then the bias voltage to start a phase for biasing the second addressing circuit; the phase for activating the first addressing circuit is synchronous with the phase for biasing the second addressing circuit, and the phase for activating the second addressing circuit is synchronous with the phase for biasing the first addressing circuit;

- the control means include selection control means including:
  - for each first addressing circuit for a light emitter, a first selection switch intended to drive the transmission of said addressing voltage or of said bias voltage, as a function of a selection voltage, to said first storage capacitor and said gate of said first current modulator in order to select said light emitter;
  - for each second addressing circuit for the same light emitter, a second selection switch intended to drive the transmission of said addressing voltage or of said bias voltage, as a function of said selection voltage, to said second storage capacitor and said gate of said second current modulator in order to select said light emitter; and
  - means for driving the first and second selection switches;
- the driving means additionally include for each row of light emitters, a first and a second selection electrode connected respectively to the first and to the second selection switches in order to control them, and a selection driving unit intended to transmit, alternately, first said selection voltage to said first selection electrode, then said selection voltage to said second selection electrode;

- the addressing control means include an addressing electrode for each column of light emitters, the first and the second selection switches being connected to said addressing electrode, and an addressing driving unit intended to send, alternately, said addressing voltage and said bias voltage to said addressing electrode;
- the driving means additionally include a selection electrode for each row of light emitters, the first and second selection switches being connected to said selection electrode in order to control them, and a selection driving unit intended to send said selection voltage concomitantly to the first and second selection switches;
- the addressing control means include for each column of light emitters, a first and a second addressing electrode connected respectively to the first and to the second selection switches, and an addressing driving unit intended to send concomitantly on the first addressing electrode and on the second addressing electrode either said addressing voltage or said bias voltage.

Another subject of the invention is an addressing method for a display screen of this type, characterized in that it includes for the driving of each light emitter:

- a phase for activating the first addressing circuit in order to supply current to the light emitter;
- a phase for biasing the second addressing circuit in order to shift the trigger threshold voltage of the second modulator;
- a phase for activating the second addressing circuit in order to supply current to the light emitter;

- a phase for biasing the first addressing circuit in order to shift the trigger threshold voltage of the first modulator, and

the phase for activating the first addressing circuit is concomitant with the phase for biasing the second addressing circuit, and the phase for activating the second addressing circuit is concomitant with the phase for biasing the first addressing circuit.

According to particular embodiments, the display method includes one or more of the following characteristics:

- one or more phases for activating the first addressing circuit are followed by at least one phase for biasing the first addressing circuit, and one or more phases for activating the second addressing circuit are followed by at least one phase for biasing the second addressing circuit;
- the method includes:
  - an addressing programming step for said first storage capacitor by applying an addressing voltage representing an image datum to said capacitor;
  - a bias programming step for said first current modulator by applying a bias voltage to said modulator, said bias voltage having an opposite polarity to the polarity of the potential stored by the first storage capacitor;
  - a bias programming step for said second current modulator by applying said bias voltage to said modulator; and
  - an addressing programming step for said second storage capacitor by applying said addressing voltage to said capacitor;
- the bias programming step for said first current modulator is followed by the addressing programming step for the second storage capacitor, and alternately the bias programming step for said

second current modulator is followed by the addressing programming step for the first storage capacitor; and

- said bias programming step for said second current modulator is concomitant with said addressing programming step for said first storage capacitor, and said bias programming step for said first current modulator is concomitant with said addressing programming step for said second storage capacitor.

The invention will be better understood on reading the following description, given by way of example only and with reference to the drawings in which:

- Figure 1 is a schematic diagram representing a light emitter and means for controlling the emission of this light emitter of the screen according to a first embodiment of the invention;
- Figures 2A to 2F are graphs representing the change over time of various voltages and currents over the course of the addressing method executed by the device according to the invention; in particular:
- Figure 2A is a graph representing the selection voltage applied to a first selection electrode;
- Figure 2B is a graph representing the voltage applied to a second selection electrode;
- Figure 2C is a graph representing the voltage applied to an addressing electrode;
- Figure 2D is a graph representing the voltage applied across the terminals of a first storage capacitor and the voltage applied across the terminals of a second storage capacitor;
- Figure 2E is a graph representing the drain current flowing through a first current modulator and the drain current flowing through a second current modulator;

- Figure 2F is a graph representing the current flowing through a light emitter;
- Figure 3 is a schematic diagram representing a light emitter and means for controlling the emission of this light emitter of the screen according to a second embodiment of the invention;
- Figures 4A to 4F are graphs representing the change over time of various voltages and currents over the course of the addressing method executed by the device according to the second embodiment of the invention; in particular:
- Figure 4A is a graph representing the selection voltage applied to a selection electrode;
- Figure 4B is a graph representing the voltage applied to a first addressing electrode;
- Figure 4C is a graph representing the voltage applied to a second addressing electrode;
- Figure 4D is a graph representing the voltage across the terminals of a first storage capacitor and the voltage across the terminals of a second storage capacitor;
- Figure 4E is a graph representing the drain current flowing through a first current modulator and the drain current flowing through a second current modulator; and
- Figure 4F is a graph representing the current flowing through a light emitter.

The display screen according to the invention is an active matrix screen including light emitters distributed in rows and columns to form an array of light emitters.

The light emitters of the display screen are organic light-emitting diodes, known by the acronym OLED. Each of them is associated with one pixel when the screen is monochrome or with a subpixel when the screen is

polychrome. They emit a luminous intensity that is directly proportional to the current flowing through them.

Figure 1 represents means 2 for controlling the emissions of the light emitters 4 of the array according to a first embodiment of the invention. For the sake of simplicity, only the means for controlling the addressing of a single light emitter have been illustrated in this figure.

The control means 2 include a first addressing circuit 6 connected to a light emitter 4 of the array, addressing control means 8 for controlling the addressing of a column of light emitters, selection control means 10 for controlling the selection of a row of light emitters, a control system 11 and a second addressing circuit 12 also connected to a light emitter 4.

The first addressing circuit 6 includes a current modulator 14, a storage capacitor 16 and a selection switch 18.

The modulator 14 and the switch 18 are hydrogenated amorphous silicon thin film transistors. More specifically, these are n-type transistors. They include a drain, a gate and a source and are intended to have a current flow through them from their drain to their source when a voltage that is greater than or equal to their trigger threshold voltage is applied between their gate and their source.

Alternatively, p-type transistors may also be used. In that case, the transistors 14 and 18 are intended to have a current flow through them from their source to their drain.

The drain of the modulator 14 is connected to the cathode of the light emitter 4. The anode of the light emitter 4 is connected to a generator of DC voltage V_{dd} intended to supply it with power. The source of the modulator 14 is connected to a ground electrode or to a negative voltage. The gate of the modulator 14 is connected to the source of the switch 18 and to a terminal of the storage capacitor 16. The other terminal of the capacitor 16 is connected to a ground electrode. The gate of the switch 18 is connected to the selection control means 10 and its drain is connected to the addressing control means 8.

The addressing control means 8 for a column of light emitters include an addressing electrode 20 for each column of light emitters and an addressing driving unit 22. The electrode 20 is connected to the driving unit 22 and to the drain of the switch 18 of first addressing circuits 6 for a column of light emitters.

The selection control means 10 include a first selection electrode 24 and a second selection electrode 26 for each row of light emitters, and a selection driving unit 28. The first selection electrode 24 is connected to the driving unit 28 and to the gate of the switch 18 of the first addressing circuits 6 for a row of light emitters. The second electrode 26 is connected to the driving unit 28 and to the gate of the switch 38 of second addressing circuits 12 for a row of light emitters.

The control system 11 is connected to the addressing driving unit 22 and to the selection driving unit 28.

The second addressing circuit 12 includes the same components as the first addressing circuit 6, namely a

current modulator 34, a storage capacitor 36 and a selection switch 38. These components are interconnected in the same way as in the first addressing circuit 6 and will not be described in detail.

Specifically, the current modulator 34 of the second addressing circuit 12 is connected to the cathode of the light emitter 4 at node 32. The drain of the switch 38 is connected to the same addressing electrode 20 as the switch 18 and its gate is connected to the second selection electrode 26.

The control system 11 is intended to transmit digital image data and data relating to the bias voltage to the driving unit 22 and a periodic selection signal to the driving unit 28 at a predefined frequency.

The addressing driving unit 22 is intended to transmit an addressing voltage V_D representing an image datum to all the light emitters of a column via the electrode 20. The addressing driving unit 22 is also intended to apply to the electrode 20 a voltage, called the bias voltage V_p, having an opposite polarization with respect to the polarization of the addressing voltage. This voltage is a predefined negative voltage having a predetermined duration. Preferably, the bias voltage V_p is between -2 volts and -25 volts. Generally, a reverse or negative bias voltage refers to a potential difference V_{gs} between the gate and source electrodes of the modulator that is less than 0 volt: $V_{gs} < 0$ V.

The driving unit 28 is intended to apply a periodic selection voltage V_{S1}, V_{S2} to the gate of the switch 18 of the first addressing circuits 6 for a row of light emitters or to the gate of the switch 38 of the second addressing circuits 12 for the same row of light

emitters in order to enable application of the addressing voltage V_D or of the bias voltage V_p to the gate of the modulator 14 of the first addressing circuit 6 or to the gate of the modulator 34 of the second addressing circuit 12.

Figures 2A to 2F illustrate the addressing method of a display screen according to the first embodiment of the invention.

This method includes a bias programming step A for the modulator 34 of the second addressing circuit 12. The selection driving unit 28 transmits a selection voltage V_{S2} to the second electrode 26, as illustrated in Figure 2B. The selection switch 38 is unblocked by the application of this selection voltage V_{S2} to its gate.

At the same time, the addressing driving unit 22 applies a bias voltage V_p of negative polarity ($V_{gs} < 0$) to the addressing electrode 20. The bias voltage V_p is applied at the gate of the current modulator 34 and at a terminal of the storage capacitor 36. The drain current I_{d2} which was flowing through the modulator 34 to power the light emitter 4 during the previous frame now tends toward 0 during this new frame as shown by the dotted-line curve in Figure 2E.

At the same time, the storage capacitor 36 having previously stored a voltage V_D applied during the previous frame, is polarized at the bias voltage V_p, as illustrated in Figure 2D; as the dotted-line curve in this figure indicates, the storage capacitor 36 maintains this bias voltage at the gate of the modulator 34 during a biasing phase for the second addressing circuit 12 and until the end of the next programming step for the modulator 34. Steps B, C and D

together form a phase for biasing the second addressing circuit 12.

The trigger threshold voltage of the modulator 34, having undergone a shift through the application of an addressing voltage during the previous image frame, is shifted again during the biasing phase and throughout the new frame, through the application of the bias voltage V_p but in an opposite direction to its previous shift.

The bias voltage applied at the gate of the modulator 34 during the new frame has the effect of reversing the shift of its trigger threshold voltage and restoring the latter to its initial value, i.e. to the value it had before having been shifted through the application of an addressing voltage at its gate during the previous frame.

During the addressing programming step B for the modulator 14 of the first addressing circuit 6, the selection driving unit 28 generates a selection voltage V_{S1} and applies it to the first electrode 24.

At the same time, the addressing driving unit 22 transmits an addressing voltage V_{Da} representing an image datum to the addressing electrode 20. The selection switch 18, at the intersection of the addressing electrode 20 and the first selection electrode 24, is unblocked and transmits the addressing voltage V_{Da} to the modulator 14 and to the storage capacitor 16 of the first addressing circuit 6. As the addressing voltage V_{Da} is greater than the trigger threshold voltage of the modulator 14, a drain current I_{d1} is established between the drain and the source of the modulator 14 and therefore flows through the light emitter 4 as illustrated in Figure 2F. The capacitor 16

stores a potential representing the addressing voltage V_{Da} at the gate of the modulator 14 in order to maintain the luminance of the light emitter 4 over a time interval corresponding to the duration of an image frame. Thus, the light emitter 4 emits light during step C until the end of the image frame.

During steps B, C and D, it is therefore seen that the light emitter 4 is supplied with current by the first addressing circuit 6. Steps B, C and D therefore together form a phase for activating the first addressing circuit 6.

During a bias programming step D for the modulator 14 of the first addressing circuit 6, the selection driving unit 28 transmits a selection voltage V_{S1} to the first electrode 24. At the same time as applying a selection voltage, the addressing driving unit 22 applies a bias voltage V_p to the electrode 20.

The selection switch 18, at the intersection of the first electrode 24 and the addressing electrode 20, is unblocked and this time transmits the bias voltage V_p to the modulator 14 and to the storage capacitor 16. The storage capacitor is discharged and stores the charges transmitted by the bias voltage during a biasing phase E, F for the first addressing circuit 6, as illustrated in Figure 2D. The drain current I_{d1} of the previous frame stops flowing through the modulator 14. The trigger threshold voltage of the modulator 14 which has shifted and increased during the image frame will decrease during the new frame and in particular during step F.

The next image frame starts with an addressing programming step E for the modulator 34 of the second addressing circuit 12. During this step, the selection

driving unit 28 applies a selection voltage V_{S2} to the electrode 26. At the same time, the addressing driving unit 22 applies an addressing voltage V_{Db} to the electrode 20.

The switch 38 of the second addressing circuit 12 is unblocked and the addressing voltage V_{Db}, representing an image datum, is applied at the gate of the modulator 34 and at the terminal of the storage capacitor 36. A drain current I_{d2} is generated between the drain and the source of the modulator 34. This current has an amplitude that is proportional to the value of the image datum to be transmitted during this image frame. This current flows through the light emitter 4 during step F until the end of the image frame.

During steps E and F, it is therefore seen that the light emitter 4 is supplied with current by the second addressing circuit 12. Steps E and F therefore together form a phase for activating the second addressing circuit 12.

Consequently, the control system 11 and the driving units 22 and 28 control the addressing of the selection, addressing and bias voltages such that:

- an addressing voltage of positive polarity is applied at the gate of the modulator 14 of the first addressing circuit 6 in order to power the light emitter 4, and following this a bias voltage of negative polarity is applied at the gate of the modulator 34 of the second addressing circuit 12 in order to compensate for the shift of its trigger threshold voltage;
- then in the opposite manner, an addressing voltage of positive polarity is applied at the gate of the modulator 34 of the second addressing circuit 12 in order to power the light emitter 4, and

following this a bias voltage of negative polarity is applied at the gate of the modulator 14 of the first addressing circuit 6 in order to compensate for the shift of its trigger threshold voltage.

From one image frame to the other, the light emitter 4 is supplied with current in turn by the first modulator 14 during a phase for activating the first addressing circuit, and then by the second modulator 34 during a phase for activating the second addressing circuit.

The trigger threshold voltages of the modulator 14 of the first addressing circuit and of the modulator 34 of the second addressing circuit are increased and then decreased in turn at each image frame. Such a device therefore advantageously provides for compensating for the trigger threshold voltage shift of the panel's modulators.

A light emitter 4 and the means 40 for controlling its emission according to a second embodiment of the invention are represented in Figure 3.

In this embodiment, the control means 40 include first addressing circuits 6 and second addressing circuits 12 each connected to a light emitter 4 of the array, addressing control means 42 for a column of light emitters, selection control means 44 for a row of light emitters and a control system 56.

The first 6 and second 12 addressing circuits include the same components, connected in the same way as the addressing circuits described with reference to Figure 1. They are identified by the same references as in Figure 1 and will not be described hereafter.

The addressing control means 42 include an addressing driving unit 46, a first addressing electrode 48 and a second addressing electrode 50 for each column of light emitters. The first addressing electrode 48 is connected to the driving unit 46 and to the drain of the switch 18 of all the first addressing circuits 6 of a column of light emitters. The second addressing electrode 50 is connected to the driving unit 46 and to the drain of the switch 38 of all the second addressing circuits 12 of a column of light emitters.

The addressing driving unit 46 is intended to send an addressing voltage V_{D1} on the first electrode 48 and, in a concomitant manner, an addressing voltage V_{D2} on the second electrode 50.

The selection control means 44 include a selection driving unit 54 and for each row of light emitters a single selection electrode 52. The selection electrode 52 is connected to the driving unit 54, to the gate of the switch 18 of the first addressing circuits 6 and to the gate of the switch 38 of the second addressing circuits 12 of a row of light emitters.

The control system 56 is connected to the driving unit 54 and to the driving unit 46. This control system 56 is intended to transmit digital image data and data relating to the bias voltage to the driving unit 46. It is also intended to transmit a periodic selection signal to the driving unit 54.

The addressing method for a display screen according to the second embodiment of the invention is illustrated in Figures 4A to 4F.

This method includes a step G for programming the addressing of the capacitor 16 and for simultaneously

programming the bias of the modulator 34. The driving unit 46 transmits an addressing voltage V_{Da} representing an image datum to the first electrode 48 and a bias voltage V_p to the second electrode 50.

At the same time, the driving unit 54 transmits a selection voltage V_S on the selection electrode 52. The switch 18 of the first addressing circuit and the switch 38 of the second programming circuit are unblocked such that the bias voltage V_p is applied at the gate of the modulator 34 and at the terminal of a capacitor 36, and such that the addressing voltage V_{Da} is applied at the gate of the modulator 14 and at a terminal of the storage capacitor 16.

The storage capacitor 36 discharges and then charges to a negative potential equal to the bias voltage V_p. This voltage, maintained at the gate of the modulator 34 by the storage capacitor 36, aims to gradually reduce the trigger threshold voltage of the modulator 34 in particular during step H. As indicated by the dotted-line curve in Figure 4E, the drain current I_{d2} becomes zero and remains zero during step H.

The capacitor 16 charges to the potential V_{Da} and a drain current I_{d1} is established between the drain and the source of the modulator 14. The light emitter 4 is powered by the current I_{d1} during step H until the end of the image frame.

During steps G and H, the light emitter 4 is therefore supplied with current by the first addressing circuit 6; steps G and H therefore together form a phase for activating the first addressing circuit. Furthermore, during steps G and H, the bias voltage is applied at the gate of the modulator 34 in order to compensate for the shift of its trigger threshold voltage. Steps G and

H also therefore together form a phase for biasing the second addressing circuit.

During a step I for programming the addressing of the storage capacitor 36 and for simultaneously programming the bias of the modulator 14, the driving unit 46 transmits a bias voltage V_p to the first electrode 48 and an addressing voltage V_{Db} representing an image datum to the second electrode 50.

The switches 18 and 38 are opened simultaneously by applying the selection voltage V_S to the electrode 52. The bias voltage V_p is transmitted to the gate of the modulator 14 and to the terminal of the capacitor 16. The capacitor 16 discharges and then charges negatively. As indicated by the solid-line curve in Figure 4E, the drain current I_{d1} becomes zero and remains zero during step J.

During steps I and J, the bias voltage V_p is applied at the gate of the modulator 14. Steps I and J therefore together form a phase for biasing the first addressing circuit 6.

At the same time, the addressing voltage V_{Db} is applied at the gate of the modulator 34 and at a terminal of the capacitor 36. This voltage, maintained at the gate of the modulator 34 by the capacitor 36, generates a drain current I_{d2} which powers the light emitter 4 during step J and until the next programming step for a new image datum.

During steps I and J, the light emitter 4 is supplied with current by the second addressing circuit 12; these steps therefore together form a phase for activating the second addressing circuit.

Consequently, the control system 56 and the driving units 46 and 54 control the addressing of the selection, addressing and bias voltages such that:

- an addressing voltage of positive polarity is applied at the gate of the modulator 14 of the first addressing circuit 6 in order to power the light emitter 4 and simultaneously a bias voltage of negative polarity is applied at the gate of the modulator 34 of the second addressing circuit 12 in order to compensate for the shift of its trigger threshold voltage;
- then in the opposite manner, an addressing voltage of positive polarity is applied at the gate of the modulator 34 of the second addressing circuit 12 in order to power the light emitter 4 and simultaneously a bias voltage of negative polarity is applied at the gate of the modulator 14 of the first addressing circuit 6 in order to compensate for the shift of its trigger threshold voltage.

The light emitter 4 is thus supplied with the modulated current in turn by the modulator 14 and then by the modulator 34.

The first 6 and second 12 addressing circuits are activated alternately to supply current to the light emitter 4.

When the modulator 14 powers the light emitter 4, the modulator 34 is biased by applying at its gate a bias voltage corresponding to a high negative voltage in order that the trigger threshold voltage of the modulator 34, shifted during the previous phase, returns to it initial value.

Otherwise, when the modulator 34 powers the light emitter 4, the modulator 14 is biased by this same

negative bias voltage in order that its trigger threshold voltage, having previously shifted in one direction, shifts in the opposite direction. Thus, the inclusion of two addressing circuits associated with each light emitter contributes to compensating for the trigger threshold variations of the modulators of a display screen.

In the embodiments just described, it is at each image frame that switchover of the activation of one and of the other addressing circuit of the screen according to the invention takes place; it is possible, without departing from the invention, to proceed with this alternating manner not at each image frame but between series of image frames.

In the embodiments described, the biasing and activation phases are carried out simultaneously and have equal durations. As a variant, the control means are also capable controlling the modulators 14 and 34 in order that the biasing and activation phases for the first and second circuits, although carried out simultaneously, have different durations.

According to a preferred embodiment, the bias voltage applied to one or to the other modulator of a light emitter varies from one image frame to the other as a function of the addressing voltage applied to this modulator during the previous frame; preferably, this bias voltage is equal but of opposite sign to said addressing voltage of the previous frame.